



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/617,817

07/14/2003

Toshio Teraishi

03DCOAI030

5232

26071 7590 08/24/2007

JUNICHI MIMURA  
OKI AMERICA INC.  
1101 14TH STREET, N.W.  
SUITE 555  
WASHINGTON, DC 20005

EXAMINER

VELEZ, ROBERTO

ART UNIT

PAPER NUMBER

2829

MAIL DATE

DELIVERY MODE

08/24/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/617,817	<b>Applicant(s)</b> TERAISHI, TOSHIO	
	<b>Examiner</b> Roberto Velez	<b>Art Unit</b> 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 June 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 4-11 and 16-19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 12-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 June 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>07/14/2003</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-3 and 12-15 have been considered but are moot in view of the new ground(s) of rejection.

### ***Claim Objections***

2. Claims 12-15 are objected to because of the following informalities: Claim 12, Ln 12 should recite "single test signal" instead of "ingle test signal". Appropriate correction is required.
3. Claims 13-15 depending from claim 12 are objected for the same reason.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-3 and 12-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1, Ln 5, recites the claim limitation "which outputs a test result only". This limitation was not found in the written description. Applicant is welcomed to point out where in the Specification the Examiner could find support for this limitation. Claim 12, Ln 12-13, recites the claim limitation "the single test signal output lead outputting

a test signal only". This limitation was not found in the written description. Applicant is welcomed to point out where in the Specification the Examiner could find support for this limitation.

6. Claims 2-3 and 13-15 depending from claims 1 or 12 are rejected for the same reason.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Berlin et al. (US Pat. 7,132,841)*** in view of ***Van Brunt (US Pat. 4,357,703)***.

Regarding claim 12, ***Berlin et al.*** shows (Fig. 1b) a chip carrier [23], which has a user area (area where 25 and 31 are positioned) and a non-user area (area where 27, 29, 35, 33 are positioned), for mounting a LSI chip in the user area, comprising: a plurality of leads [25 on the left side], each of which is formed in the user area (area where 25 and 31 are positioned) and extended in a first direction to the non-user area (area where 27, 29, 35, 33 are positioned); a plurality of leads [25 on the right side], each of which is formed in the user area (area where 25 and 31 are positioned) and extended in a second direction, which is different from the first direction, to the non-user area (area where 27, 29, 35, 33 are positioned); a single test signal input lead (either one of 31), which is

formed in the user area (area where 25 and 31 are positioned) and extended in the first direction to the non-user area (area where 27, 29, 35, 33 are positioned); and a single test signal output lead (either one of 31), which is formed in the user area (area where 25 and 31 are positioned) and extended in the first direction to the non-user area (area where 27, 29, 35, 33 are positioned).

**Berlin et al.** fails to specify input leads, output leads, a single test signal input lead receiving a test signal for testing an internal circuit formed in the LSI chip and a single test signal output lead outputting a test signal only. However, **Van Brunt** shows (Fig. 1) input leads [12], output leads [30], a single test signal input lead [21] receiving a test signal for testing an internal circuit [11] formed in the LSI chip (Col. 4, Ln 1-5) and a single test signal output lead [33] outputting a test signal only (Col. 4, Ln 12-19).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of **Van Brunt** into the device of **Berlin et al.** by having and assigning input leads, output leads, a single test signal input lead and a single test signal output lead in the chip carrier to match a LSI chip pattern. The ordinary artisan would have been motivated to modify **Berlin et al.** in the manner set forth above for the purpose of performing dynamic testing of complex logic modules in an efficient and faster manner.

Regarding claim 13, the combination of **Berlin et al.** and **Van Brunt** discloses everything as claimed above in claim 12; in addition, **Berlin et al.**

shows (Fig. 1b) a plurality of test pads [35] formed in the non-user area (area where 27, 29, 35, 33 are positioned).

**Berlin et al.** fails to disclose each of which is connected to one of the output leads. However, **Van Brunt** shows (Fig. 1) a test pad (will be connected to 33) connected (electrically connected) to each one of the output leads [30].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of **Van Brunt** into the device of **Berlin et al.** by having a plurality of test pads formed in the non-user area, each of which is connected to one of the output leads. The ordinary artisan would have been motivated to modify **Berlin et al.** in the manner set forth above for the purpose of having alternate paths to transmit test signals.

Regarding claim 14, the combination of **Berlin et al.** and **Van Brunt** discloses everything as claimed above in claim 12.

The combination of **Berlin et al.** and **Van Brunt** fails to disclose wherein a width of the test signal output lead is wider than that of each output lead.

It would have been obvious to have a wider test signal output lead than that of each output lead for the purpose of minimizing alignment error tolerance while making contact between the test signal output lead of the carrier and the test signal output terminal of the LSI chip.

Regarding claim 15, the combination of **Berlin et al.** and **Van Brunt** discloses everything as claimed above in claim 12.

The combination of *Berlin et al.* and *Van Brunt* fails to disclose wherein a test signal input lead and the test signal output lead sandwich the input leads.

It would have been obvious to sandwich the input leads with the test signal input lead and the test signal output lead for the purpose of making easier to manufacture.

### **Conclusion**

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
10. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.
11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-

Art Unit: 2829

272-8597. The examiner can normally be reached on Monday-Friday 8:00am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Roberto Velez  
Patent Examiner

  
HA TRAN NGUYEN  
SUPERVISORY PATENT EXAMINER

8/20/7